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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/775,262

02/10/2004

Scott E. Post

DP-309692

1256

7590

03/25/2005

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EXAMINER

NORRIS, JEREMY C

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/775,262

Applicant(s)

POST ET AL.

Examiner

Jeremy C. Norris

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2-10-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

- (1) if a machine or apparatus, its organization and operation;
- (2) if an article, its method of making;
- (3) if a chemical compound, its identity and use;
- (4) if a mixture, its ingredients;
- (5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the use of the phrase "is provided". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-9, 11, 12, and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,275,330 (Isaacs).

Examiner notes that the "drilling" and "plating" manufacturing steps claimed are process limitation in a device claim and thus are only considered to the extent to which they impact the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)).

Isaacs discloses, referring primarily to figure 9, an electronic package comprising: a circuit board having a substrate (10) and circuitry (18, 20, 22); a surface mount device (44) having a contact terminal (40); a mounting pad (12) formed on the circuit board; a plurality of vias (16) extending into the circuit board and the mounting pad, each of the vias having an opening extending therein; and a solder joint (46, 31) connecting the contact terminal of the surface mount device to the mounting pad on the circuit board, wherein the solder joint extends at least partially into the opening in each

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of the plurality of vias to support the arrangement of the surface mount device on the circuit board [claim 1], wherein the plurality of vias comprise a plurality of electrically conductive vias electrically coupled to the circuitry on the circuit board [claim 2], wherein the circuit board comprises an organic substrate (see col. 4, lines 50-55) [claim 4], wherein the circuit board comprises a printed circuit board (see col. 4, lines 50-55) [claim 5], wherein the solder joint comprises solder reflowed at an elevated temperature to at least partially fill each of the plurality of vias to form a column within each of the vias (see col.5, lines 30-40) [claim 6], wherein the package includes first and second mounting pads each having a plurality of vias extending into the circuit board and each containing a column of the solder joint for supporting the surface mount device on the circuit board (see figure 9) [claim 7], wherein the surface mount device comprises an electronic device having electrical circuitry (see col. 6, lines 35-50) [claim 8], wherein each of vias are formed by drilling an opening and plating the opening with an electrically conductive material (see col. 4, lines 50-60) [claim 9].

Similarly, Isaacs discloses, an electronic package comprising: a circuit board having a substrate (10) and circuitry (18, 20, 22); a surface mount device (44) having a contact terminal (40); a mounting pad (12) formed on the circuit board; a via (16) extending into the circuit board and extending through the mounting pad, said via having an opening extending therein; and a solder joint (46, 31) connecting the contact terminal of the surface mount device to the mounting pad on the circuit board, wherein the solder joint extends at least partially into the opening in the via to form a solder column that supports the arrangement of the surface mount device on the circuit board

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[claim 11], wherein the via comprises an electrically conductive via electrically coupled to the circuitry on the circuit board (see col. 5, lines 1-10) [claim 12] wherein the circuit board comprises an organic substrate (see col.4, lines 50-60) [claim 14], wherein the circuit board comprises a printed circuit board (see col. 4, lines 50-60) [claim 15], wherein the solder joint comprises solder reflowed at an elevated temperature to at least partially fill the via to form a column within the via (see col. 5, lines 30-40) [claim 16], wherein the via comprises first and second vias extending through the mounting pad and into the circuit board, wherein the solder joint has a column extending at least partially into each of the first and second vias to further support the arrangement of the surface mount device on the circuit board (see figure 9) [claim 17], wherein the package includes first and second mounting pads, each having a via extending into them through and the circuit board and each receiving solder for supporting the surface mount device on the circuit board (see figure 9) [claim 18], wherein the via is formed by drilling an opening into the circuit board and plating an electrically conductive material in the opening (see col. 4, lines 50-60) [claim 19], wherein the surface mount device comprises an electronic device having electrical circuitry (see col. 6, lines 35-50) [claim 20].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacs in view of US 5,489,750 (Sakemi).

Isaacs discloses the claimed invention as described above except Isaacs does not specifically state that the plated through holes comprise copper [claims 3, 13].

However, it is well known in the art to use copper as through hole plating as evidenced by Sakemi (see col. 5, lines 10-20). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use copper as the plating

metal in the vias in the invention of Isaacs. The motivation for doing so would have been to take advantage of the high electroconductivity and relatively low cost of copper. Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Claims 10 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacs in view of US 6,083,834 (Chang).

Isaacs discloses the claimed invention as described above except Isaacs does not specifically state that, wherein the package has an aspect ratio of circuit board thickness to diameter of the opening of each of the vias of no greater than about 5.0. [claims 10, 21] However, it is well known in the art to form vias having an aspect ratio of no greater than about 5 as evidenced by Chang (see col.1, lines 20-40). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use an aspect ratio of less than 5 for the vias in the invention of Isaacs as is well known in the art and evidenced by Chang. The motivation for doing so would have been to choose a via size that is more easily formed and filled with the solder material (see Chang, col. 1, lines 25-30).

Conclusion

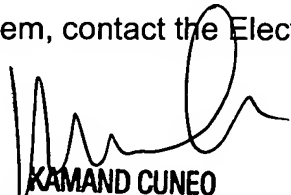
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose PCBs having SMT devices:

US 6,472,610	Kawabata,
US 6,509,530	Pearson et al.,
US 6,735,857	Saito et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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